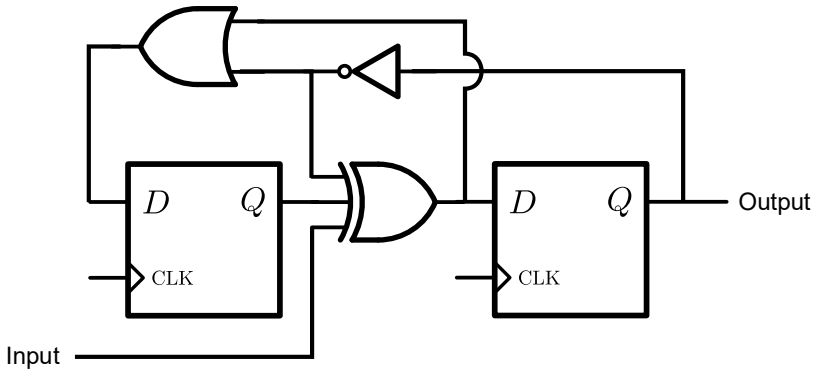
(2) Synchronous Digital System Question

$t_{\text{period}} = 20\ ns, t_{\text{setup}} = 2\ ns$

$t_{\text{XOR}} = t_{\text{OR}} = 5\ ns, t_{\text{NOT}} = 4\ ns$

Input changes 1 ns after clock trigger

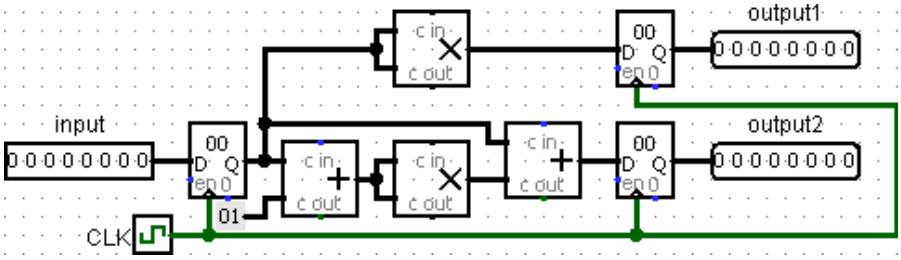


A) What is the max t_{C2Q}?

B) If $t_{\text{C2Q}} = 3\ ns$, what is the max t_{hold}?

(1) Practice question

We want to run our CPU at 1 GHz. Assume t_{add} = 100 ps. t_{mult} = 200 ps. t_{setup} = t_{hold} = 50 ps. What is the maximum $t_{clk\text{-}to\text{-}q}$ we can allow?



(3) More SDS practice

For an n-bit ripple-carry adder, what is the shortest and longest time that output S changes after each clock cycle?

- Assume A, B, c_0 straight from register output (eg, change at t_{C2Q})
- Assume all gates have a delay of 1 ns

